REMARKS

This communication is responsive to the Official Action dated October 1, 2003.

Claims 45-72 were pending in the application.

No claims were allowed.

No changes are made to the claims.

Accordingly, claims 45-72 are currently pending in the application.

Request for Continued Examination:

This communication is filed in connection with a concurrent request for continued examination.

Brief Discussion of the Invention:

Before discussion the claim rejections, a review of the inventive subject matter is believed to be in order. The claimed inventions in this application address a problem that can occur in the packaging of VCSELs and other surface normal optoelectronic devices that has not been addressed in the prior art. One of the major advantages of VCSELs as lasers is the fact that they can be tested and characterized on-wafer to determine their suitability for packaging. This can be a great cost advantage.

Unfortunately, some packaging procedures, such as solid material encapsulation, necessarily change the device characteristics of typical VCSELs, making it difficult to predict the performance of packaged devices from the on-wafer performance. The Examiner should note that the term encapsulation as used within the present specification is intended to mean a solid optically transmissive encapsulation material that is molded over the VCSEL device. The changes in the device characteristics that occur when encapsulated, occur as a result of the interface between the surface of the VCSEL and the surface of the encapsulation material rather than air.

Continuing with the noted limitation that the device is encapsulated, a question then arises. Can the devices be fabricated in such a way as to make the on-wafer performance the same as the packaged (encapsulated) performance? This application presents a totally non-

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obvious affirmative answer to that question. *Surprisingly, the deposition of a pre-calculated thickness of just one extra layer of optically transparent material, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror, so as to make the on-wafer performance the same as the packaged performance.*

Claim rejections under 35 USC §102:

Claims 45-50 and 67-69 were rejected under 35 USC §102(a) as being anticipated by Jian (USP 6,328,482).

As a basis for the rejection, the Examiner stated the following:

> *"With respect to claims 45 and 48, figure 6 shows an optical fiber transmitter comprising VCSEL 600 integrated with a fiber coupler in a single structure; a substrate with electrical interconnect 630,640; VCSEL 600 includes a surface normal optical device on said substrate; optical fiber transmitter device comprising a plurality of layers including an optically transparent (130,140,603) encapsulation medium matching layer , said medium matching layer having a different index of refraction n1 and n2; said medium matching layer having a predetermined thickness configured to adjust an optical characteristic of said opto-electronic device so as to make pre-encapsulation on-wafer test characteristics similar to post encapsulation performance characteristics (note column 10).*
>
> *With respect to claims 46-47 and 49-50, Figure 6 shows the optical device comprising a VCSEL (600).*
>
> *With respect to claims 67-69, Jian discloses a method of fabricating an encapsulated opto-electronic device ...(note Col. 6, line 16 to Col. 9 line 24 and Figures 1-4) ."*

Claims 51-66 and 70-72 were rejected under 35 USC §102(b) as being anticipated by Kopf et al (USP 5,115,441).

> *With respect to claims 51, 59 and 70, Kopf discloses a VCSEL structure (10) comprising a substrate (12), a first mirror (13) overlying said substrate, an*

active optical region (15) overlying said first mirror; a second mirror overlying said active optical region; and an optical transparent (23) encapsulation medium matching layer deposited onto said VCSEL structure and overlying said second mirror, said medium matching layer having a different index of refraction; said medium matching layer having a predetermined thickness configured to adjust reflectivity of said second mirror so as to make pre-encapsulation on wafer test characteristics of said VCSEL substantially similar to post encapsulation functional characteristics (Note Col. 3 , line 1 to Col. 8. line 14 and Fig. 1).

With respect to claims 52-58, 60-66 and 71-72, Kopf discloses a tuning layer in one of a plurality of layers of a DBR lying between said second mirror and said medium matching layer (note Col. 3, line 1 to Col. 8, line 14 and Figs. 1-5)."

Applicant's previous arguments with respect to claims 45-72 were considered but are moot in view of the NEW grounds of rejection. Applicant's amendments necessitated the NEW grounds of rejection.

The examiner has declared that previous arguments are moot in view of the new ground(s) of rejection. However, the majority of those arguments and the explanations of the main points of our application, are still very relevant to the new cited art and are repeated again herein.

The claimed inventions in this application address a problem that can occur in the packaging of VCSELs that has not been addressed in the prior art, including Jian (US patent 6,328,482) and Kopf et al (US patent 5,115,441). One of the major advantages of VCSELs as lasers is the fact that they can be tested and characterized on-wafer to determine their suitability for packaging. This can be a great cost advantage. **Unfortunately, some packaging procedures, such as encapsulation, necessarily change the device characteristics of typical VCSELs, making it difficult to predict the performance of packaged devices from the on-wafer performance.** A question then arises. Can the devices be fabricated in such a way as to make the on-wafer performance the same as the packaged

performance? This application presents a totally not obvious affirmative answer to that question. *Surprisingly, the deposition of a pre-calculated thickness of just one extra layer of optically transparent material, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror, so as to make the on-wafer performance the same as the packaged performance.* We call this layer the medium-matching layer. Then, a second important question arises. Can the devices be fabricated in such a way as to not only make the on-wafer performance the same as the packaged performance, but to make both conform to tight predetermined specifications? Once again, this application presents a totally not obvious affirmative answer. *The deposition of a pre-calculated thickness of two different extra layers of optically transparent materials, atop the VCSEL, can adjust the reflectivity of the top VCSEL mirror; so as to make the on-wafer performance the same as the packaged performance, with both conforming to tight predetermined specifications.* Below is a detailed explanation of how the medium-matching layer functions and then how that medium-matching layer functions with a tuning layer just under it.

VCSEL mirrors are Distributed Bragg Reflectors (DBR's), consisting of alternating layers of materials with different indices of refraction, with each layer a quarter-wave thick. Each interface, where the index changes, partially reflects an incident beam by an amount given by the equation, $R = (n_1 - n_2)^2 / (n_1 + n_2)^2$. The quarter-wave thickness of each layer is a phase-matching thickness, causing all the partial reflections to enjoy completely constructive interference, maximizing the reflectivity for the given number of interfaces.

The last interface is between the last mirror layer and the medium into which the VCSEL launches light, which is usually air with an index of refraction ≅ 1 (it is air during on-wafer testing). This last interface always makes a significant contribution to the total reflectivity of the top mirror. The reflectivity of the last interface depends only on the index of the last mirror layer and on the index of the medium, although the medium is not per se a part of the VCSEL structure. It does not depend on what is beneath the last layer, so for simplicity of discussion one can analyze the situation while having no other layers or interfaces below the last interface, making it the only interface between a substrate (with an index, n_s) and a medium (with an index, n_m) as is shown in Exhibit 1. If one changes the medium, as one does by encapsulating a device, then one necessarily changes the reflectivity of the last interface (as

is shown in Exhibit 1), and in a VCSEL, one thereby changes the total reflectivity of a top mirror and so changes the device performance. This result appears to be inescapable.

The first primary invention (the medium-matching layer) described in our application, and again illustrated in the attached Exhibit 2, first of all recognizes that the last mirror layer (or equivalently the substrate in Exhibit 2) can be covered by an additional layer to create two last interfaces, whose reflectivities need to be analyzed in tandem. The reflectivity of that pair of interfaces is a function of the reflectivities of each interface and of the phase angle between them, given by "k*d" (where d is thickness of the additional layer, and k is defined in Exhibit 2). The exact relationship is shown in Exhibit 3. At first sight, it appears that this is no solution. As the medium (that is the index of the medium) is changed, although the reflectivity of the lower interface does not change, the reflectivity of the upper interface does change, and to compensate for that change so as to keep the reflectivity of the tandem the same, it appears that one needs to change the phase angle, that is to change the thickness, d, of the additional layer, or its index (to change k). The second significant, unexpected insight in our application and the core of the first primary invention, is that for layers with a certain k, one can find a thickness, d, and thus a single phase angle "k*d", which yields the same reflectivity for the tandem of two interfaces, for two different mediums. Thus, for instance, such a "medium-matching" layer can yield the same reflectivity whether the medium is air, with an index, $n_a \cong 1$, or any encapsulant, with an index n_m. Most noteworthy is the fact that, in practice, this "medium-matching" layer can be and should be deposited during wafer-level device fabrication prior to on-wafer testing. Thus, all the devices on the wafer will already have the same characteristics during the on-wafer testing, as they will after they are packaged with an encapsulation. The "medium-matching" layer is not deposited or attached during the packaging procedure because by then it is too late, since the on-wafer testing was completed beforehand.

Even though the "medium-matching" layer yields the same reflectivity and thus the same performance for a device in two different mediums, it may not yield the "desired" reflectivity and performance. *The second important invention in this application is that a tuning layer can be placed between the last mirror layer and the "medium-matching" layer.*

so as to adjust the reflectivity to a particular value, which remains the same in two different mediums. Scott et al (US patent 6,392,256) and a patent application cited therein ("Vertical Cavity Surface Emitting Lasers with Consistent Slope Efficiencies", Application No. 09/237,580) disclose the use of a tuning layer, but only with it alone deposited on the last layer of the top mirror of a VCSEL, as shown in the attached Exhibit 4. Since the "medium-matching" layer and the tuning layer affect each other and each other's function, it is not obvious that they can be effectively combined. Also, their designs need to be different when combined than when separately deployed.

In Figure 6, of Jian (US patent 6,328,482) none of the layers play the role of a "medium-matching" layer. Layer 603 is the wafer substrate with an aligned micro-lens 605. This combination is made during wafer level device fabrication, but the reflection from the surface of the micro-lens will be different before and after the other layers are attached, and thus the combination is not a "medium-matching" layer. The addition of the epoxy layer 650 and the AR layer 612 does not change the situation, even though they also can be added during wafer level device fabrication. There will be a reflection from the external surface into air and no reflection into the glass layer 140, which can be considered the packaging medium, once it is attached. Since the glass layer 140 cannot be attached at wafer level except with enormous difficulty it should not be considered the "medium-matching" layer, to layer 130 as the medium. Even if it were attached at wafer level, there is no mention in Jian (US patent 6,328,482) of any specification to its thickness, to make it a "medium-matching" layer. In fact, the patent nowhere alludes to the problem that "medium-matching" layer solves, or how to solve the problem. The layer 130 can only be considered as a different medium than air, and the interface at 132/141 has no "medium-matching" layer. Very similar arguments apply to the embodiments in figures 5&7 of Jian (US patent 6,328,482). Therefore, it is submitted that this patent, Jian (US patent 6,328,482) in no way anticipates any claims in our application.

In Figure 1, of Kopf et al (US patent 5,115,441) none of the layers play the role of a "medium-matching" layer. The only layers in Figure 1, which could even be considered as "medium-matching" layers, are layers 20, 21, 22 and 23, as they are the only layers that appear above the top mirror. Layer 20 is a dielectric layer into which a window, 21, is etched. Being

a window, a hole in layer 20, feature 21 is not even a layer, so it cannot be the "medium-matching" layer. Since layer 20 is etched away in the region through which the light passes, it also cannot be the "medium-matching" layer, since it does not exist in the path of the light. Layer 22 is a barrier metal layer, deposited, as it is stated in that patent (column 5, lines 25-40), for its electrical and not for its optical characteristics, and it does not have any characteristics that could even allow it to play the role of a "medium-matching" layer. Finally, the layer 23 (column 4, line 61 to column 5, line 24) is an optically transparent electrode. Its purpose is "to serve as the vertical injection contact without substantially interfering with the light output". There is no mention in Kopf whatsoever as to how this layer could be a "medium-matching" layer. The other figures in Kopf only show device characteristics and no alternative embodiments. In fact, the patent nowhere alludes to the problem that "medium-matching" layer solves, or how to solve the problem. Accordingly it is submitted that Kopf et al (US patent 5,115,441) does not anticipate any claim in our application.

Withdrawal of the Section 102 rejections, and review and reconsideration of claims 45-72 is respectfully solicited.

Accordingly, claims 45-72 are believed to define patentable subject matter in view of the prior art cited.

Claims 45-72 are thus believed to be in condition for allowance and the application now ready for issue.

Corresponding action is respectfully solicited.

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PTO is authorized to charge any additional fees incurred as a result of the filing hereof or credit any overpayment to our account #02-0900.

Respectfully submitted,

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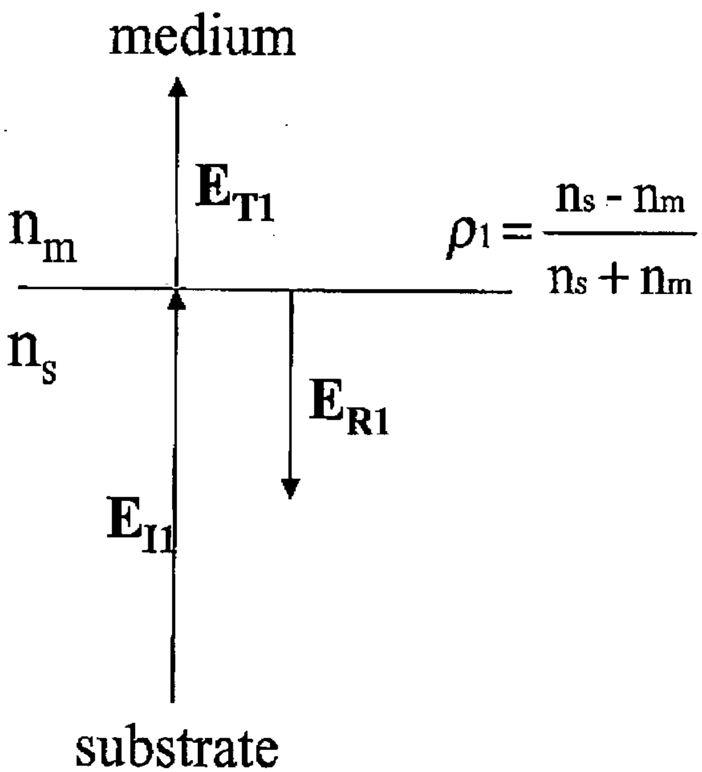
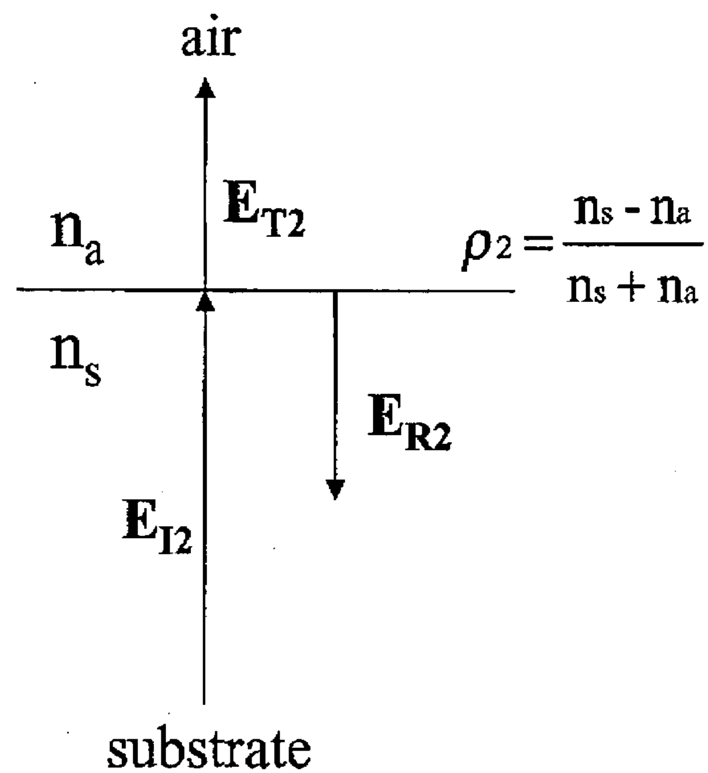
$$R_1 = (\rho_1)^2$$
$$T_1 = 1 - R_1$$

$$R_2 = (\rho_2)^2$$
$$T_2 = 1 - R_2$$





NOTE: $R_1 \neq R_2$ & $T_1 \neq T_2$, because $n_m \neq n_a$

Exhibit 1. Elementary Example of the Problem

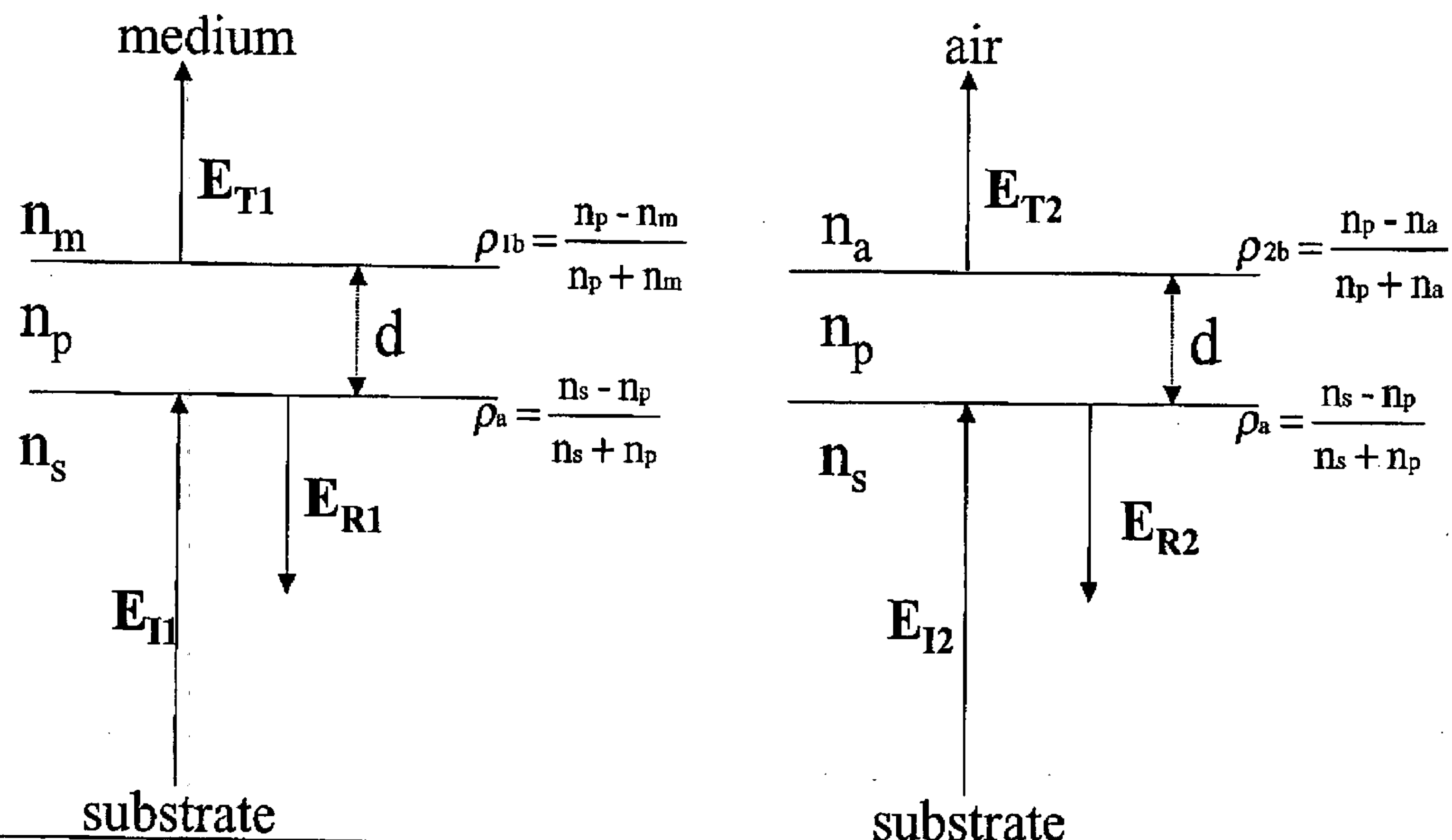
$R_1 = f(\rho_{1b}, \rho_a, k, d)$

$T_1 = 1 - R_1$

$R_2 = f(\rho_{2b}, \rho_a, k, d)$

$T_2 = 1 - R_2$

$$k = \frac{2\pi n_p}{\lambda}$$



Not obvious: there is a "d" $\ni$ $R_1 = R_2$ & $T_1 = T_2$, though $n_m \neq n_a$

Exhibit 2. Elementary Example of the Solution

$$R_1 = \frac{(\rho_a + \rho_{1b})^2 - 4\rho_a \rho_{1b} \sin^2 kd}{(1 + \rho_a \rho_{1b})^2 - 4\rho_a \rho_{1b} \sin^2 kd}$$

$$R_2 = \frac{(\rho_a + \rho_{2b})^2 - 4\rho_a \rho_{2b} \sin^2 kd}{(1 + \rho_a \rho_{2b})^2 - 4\rho_a \rho_{2b} \sin^2 kd}$$

Exhibit 3. Formulas for the R1 & R2 in Exhibit 4

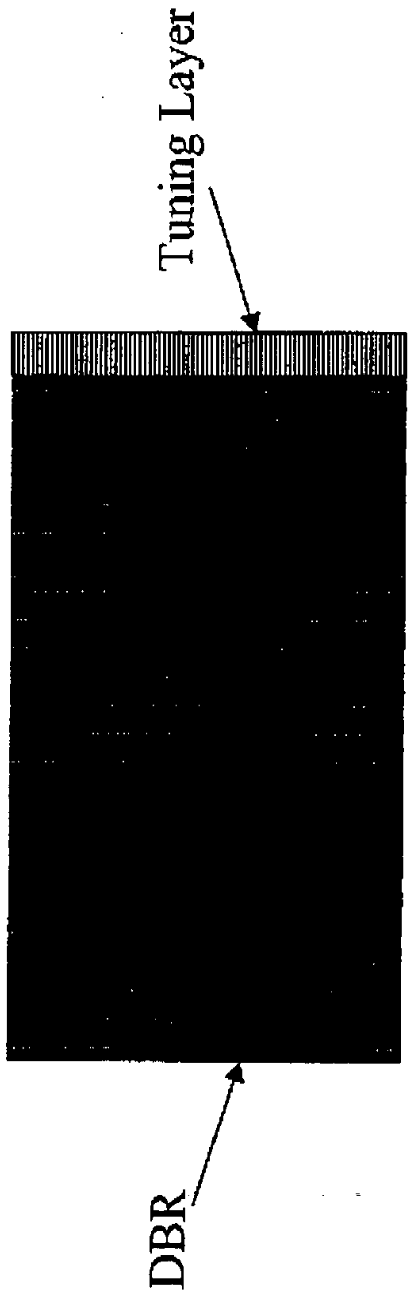


Exhibit 4. Prior Art Tuning Layer